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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,964	03/11/2004	Gunter Willy Steinbach	10031355-1	6281

7590 06/03/2005

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EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,964	STEINBACH ET AL.	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8-11,14,16-19 and 21* is/are rejected.

7)☒ Claim(s) *3-7,12,13,15 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-11-04*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 8-11, 14, 16-19 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by the DeVito reference (US Patent 6,466,096).

DeVito discloses in figure 1 a phase locked loop comprising a step size controller (22, 24 and 36) configured to provide a first VCO control signal (coarse tune) to the VCO 26 upon establishing frequency lock, said first VCO control signal causing the VCO frequency to change by a first step size (col. 4, lines 41-47); and provide a second VCO control signal (fine tune) to the VCO some time after the VCO frequency has changed in response to the first VCO control signal (col. 4, lines 48-50), said second VCXO control signal causing the VCO frequency to change by a second step size, wherein the first step size is larger than the second step size (i.e., coarse tune defines a specified frequency range and fine tune adjusts a frequency to be identical to the frequency of the input data) as required by claim 11.

As to claim 14, the output of phase detector 20 is seen as a control signal to indicate frequency lock and to provide the second VCO control signal.

As to claims 1 and 2, they are rejected for reciting method derived from an apparatus of claim 11. It is noted that the first step size (coarse tuning) is larger than the second step size (fine tuning). Therefore, the first step size provides a faster VCO pull in rate than the second step size.

As to claim 8, it is rejected for reciting a method derived from an apparatus of claim 14 which is rejected as noted above.

As to claim 9, loop filter 22 in figure 1 delays the control signal (i.e., output of 20) that indicates frequency lock.

As to claim 10, col. 3, lines 62-64 imply that the first and second step sizes are programmable.

As to claim 16, DeVito discloses in figure 1 a system for controlling a VCO 26 in a PLL circuit, the system comprising timing control logic (36, 38) configured to control the timing of changes in VCO frequency step size in response to a control signal (output of 32) that indicates frequency lock; and step size logic (20,22,24) in signal communication with the timing control logic configured to change the VCO frequency step size from a first step size (coarse) to a second step size (fine) in response to a timing control signal (output of 38) from the timing control logic, wherein the first step size is larger than the second step size (i.e., coarse tune defines a specified frequency range and fine tune adjusts a frequency to be identical to the frequency of the input data) as required by claim 16.

As to claim 17, col. 5, lines 50-52, discloses element 38 being a filter which is qualified to be considered a delay logic for generating the timing control signal by delaying he control signal that indicates frequency lock.

As to claim 18, loop filter 22 is seen as a DAC converter for converting digital step size signals (output of phase detector 20) into an analog step size signal.

As to claim 19, figure 1 also shows the step size logic (20,22,24) being configured to output a step size signal to the VCO, which sets the VCO frequency step size.

As to claim 21, col. 3, lines 62-64 imply that the first and second step sizes are programmable.

Allowable Subject Matter

3. Claims 3-7, 12-13, 15 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus and method thereof comprising elements being configured as recited in claims. Specifically, none of the prior art teaches or fairly suggests, among other things, the limitation "*limiting the time during which the VCO frequency is changed by the first step size*" as required by claims 3 and 12; "*changing the VCO frequency by the second step size through at least one intermediate step size intermediate between said first and second step sizes*" as required by claims 4 and 13; "*timing control logic configured to control the timing of transitioning from the first VCO control signal to the second VCO control signal in response to a control signal that indicates frequency lock; and step size logic in signal communication with the timing control logic configured to transition from the first VCO control signal to the second VCO control signal in response to a timing control signal from the timing control logic*" as required by claim 15; and "*the step size logic includes an up/down counter and a comparator, the comparator being configured to compare a counter value from the counter with a programming input and to output a signal that causes the up/down counter to increment or decrement in response to the comparison*" as required by claim 20.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
5-18-05

TIMOTHY P. CALLAHAN
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